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10/626,756	07/24/2003	Kevin Traynor	032674-200	1739

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EXAMINER
DANG, KHANH

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 10/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/626,756	TRAYNOR ET AL.	
	Examiner	Art Unit	
	Khanh Dang	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Notice to Applicants

This application, previously assigned to and examined by Ex. Justin King, is now assigned to Ex. Khanh Dang. Any further communication should be directed to Ex. Khanh Dang whose contact information can be found at the end of this Office Action.

All previous rejections set forth in the previous Office Action have been withdrawn.

New grounds of rejections are provided below:

Claim Rejections - 35 USC § 112

Claims 7-20 and 23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 7-13 are directed to an apparatus. However, the essential structural cooperative relationship(s) between the so-called "logic that maps," "logic that selectively enables," "logic that determines," "logic that advances," "logic that sets," "logic that dynamically modifies," and "logic that defines" have been omitted, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

Claims 14-20 are directed to an apparatus. However, the essential structural cooperative relationship(s) between the so-called "plurality of logical ANDs" and "logical

OR" have been omitted, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

Claim 23 is also directed to an apparatus. However, the essential structural cooperative relationship(s) between the so-called "logic that maps" and "logic that selectively enables" have been omitted, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

MPEP 2172.01 requires that relationships between elements recited in the claims must be specified. Specifically, MPEP 2172.02 requires interrelation and structural relationships between essential elements in the claims. Therefore, it is the Examiner's position that the claimed elements, as defined in the originally filed specification and as identified above, are essential elements to the claimed invention. Since they are essential elements as defined in the originally filed specification, their structural cooperative relationships must be provided in the claims. Further, it is also the Examiner's position that the claimed elements, as identified above, function simultaneously, are directly functionally related, directly inter-cooperate, and/or serve independent purposes, as evidenced from the originally filed specification.

If Applicants disagree with the Examiner that the above identified elements, as defined by the originally filed specification, are essential elements to the claimed invention, and that the above identified elements are directly functionally related, directly inter-cooperate, and/or serve independent purposes, it is requested that Applicants provide evidences showing that the identified elements are not essential elements to the claimed invention, do not function simultaneously, are not directly

functionally related, do not directly inter-cooperate, and/or do not serve independent purposes; and state for the record that this is the case.

Further, in new claim 22, line 7, "the same interrupt source" lacks antecedent basis. It is unclear which "source" the term "the same interrupt source" may refer to. Further, the phrase, the language such as "the same interrupt source is enabled ... the plurality of interrupts" is unclear and cannot be ascertained in view of the originally filed specification. According to Applicants' disclosure, it is the interrupts request originated from an interrupt source; and such a request can be enable or disabled depending from the setting of a control bit.

Likewise, in new claim 23, "the same interrupt source" lacks antecedent basis. It is unclear which "source" the term "the same interrupt source" may refer to. Further, the phrase, the language such as "the same interrupt source is enabled ... the plurality of interrupts" is unclear and cannot be ascertained in view of the originally filed specification. According to Applicants' disclosure, it is the interrupts request originated from an interrupt source; and such a request can be enable or disabled depending from the setting of a control bit.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 7, new claim 21, and new claim 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Armstrong (5,764,996).

As broadly drafted, claims 1, 7, 21, and 23 do not define any structure/step that differs from Armstrong. As a matter of fact, by drafting claims 1, 7, 21, and 23, Applicants are attempting to claim the notoriously well-known interrupt sharing architecture defined by the PCI Local Bus Specification, as described in Fig. 2 of Armstrong, and specifically disclosed in column 1, lines 37-43 and column 2, lines 56-67.

With regard to 1, Armstrong discloses that method for sharing a plurality of interrupt inputs associated with a processor among a plurality of interrupt sources, comprising the steps of: mapping each of the plurality of interrupt sources to each of the plurality of interrupt inputs; and selectively enabling interrupt requests from each of the plurality of interrupt sources to one or more of the plurality of interrupt inputs (Armstrong discloses that, according to the PCI Local Bus Specification adopts a shared or wired-OR interrupt binding architecture. As shown in Fig. 2:

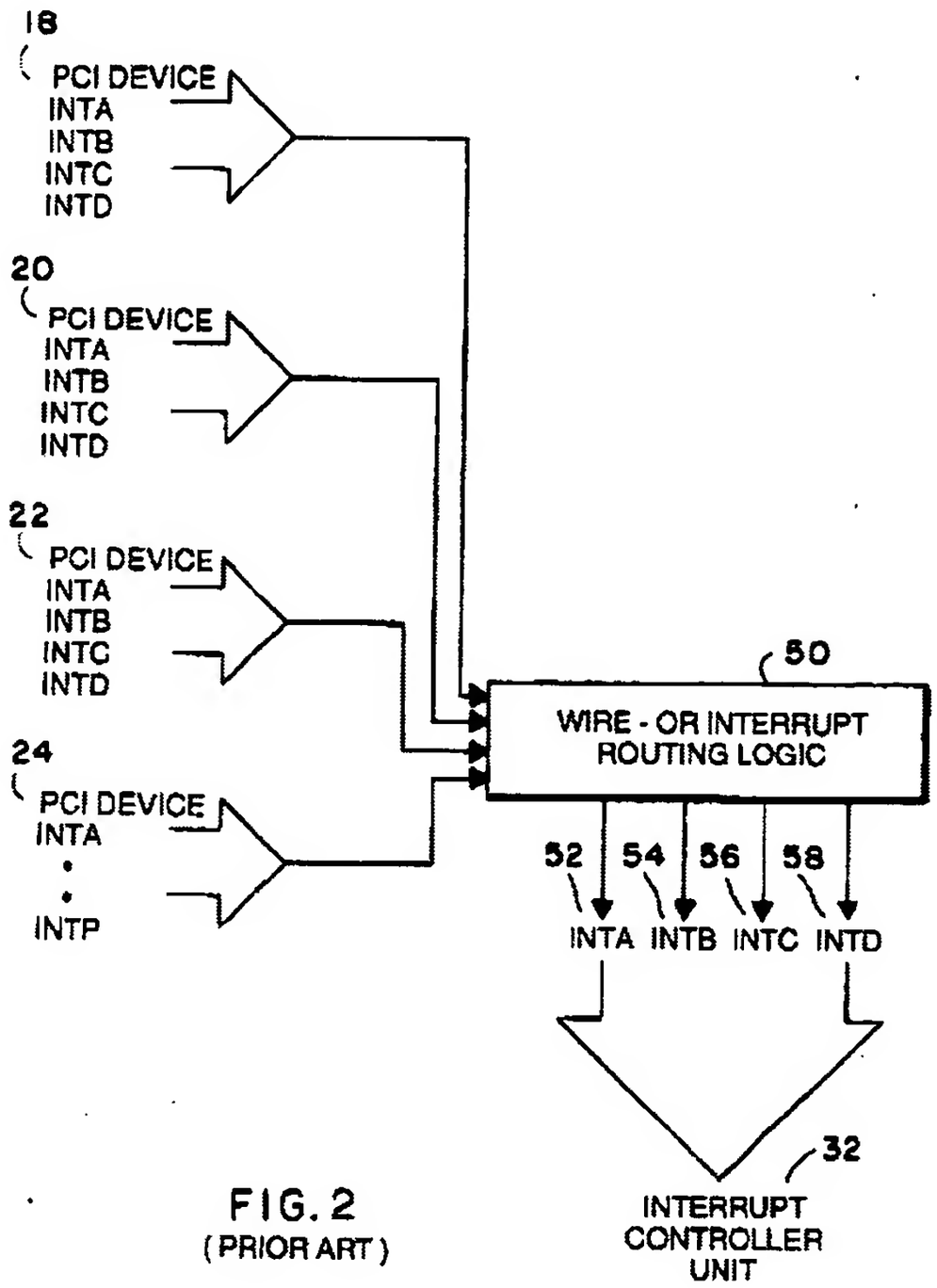
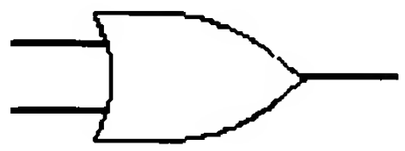


FIG. 2
(PRIOR ART)

all PCI interrupt sources are wired-OR'ed in the wired-OR interrupt routing logic 50 to map into interrupt inputs INTA – INTD of the interrupt controller 32. As well-defined in computer architecture, the logic OR gate selectively enable an output based on values of the 2 inputs:



OR gate

Input 1	Input 2	Output
0	0	0
0	1	1
1	0	1
1	1	1

Thus, it is clear that the wired-OR serves as a decision making unit to selectively enable PCI interrupt requests from each of the plurality of PCI interrupt sources to one or more of the plurality of interrupt inputs INTA – INTD of the interrupt controller 32.

With regard to claims 7, 21, and 23, see discussion above, since the subject matter presented in these claims has already been addressed.

Claims 1-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Wach (5,530,875).

With regard to claim 1, Wach discloses a method for sharing a plurality of interrupt inputs associated with a processor among a plurality of interrupt sources, comprising the steps of: mapping each of the plurality of interrupt sources to each of the plurality of interrupt inputs; and selectively enabling interrupt requests from each of the plurality of interrupt sources to one or more of the plurality of interrupt inputs (Wach

discloses an interrupt architecture employing interrupt sharing, which is best illustrated in the following figure:

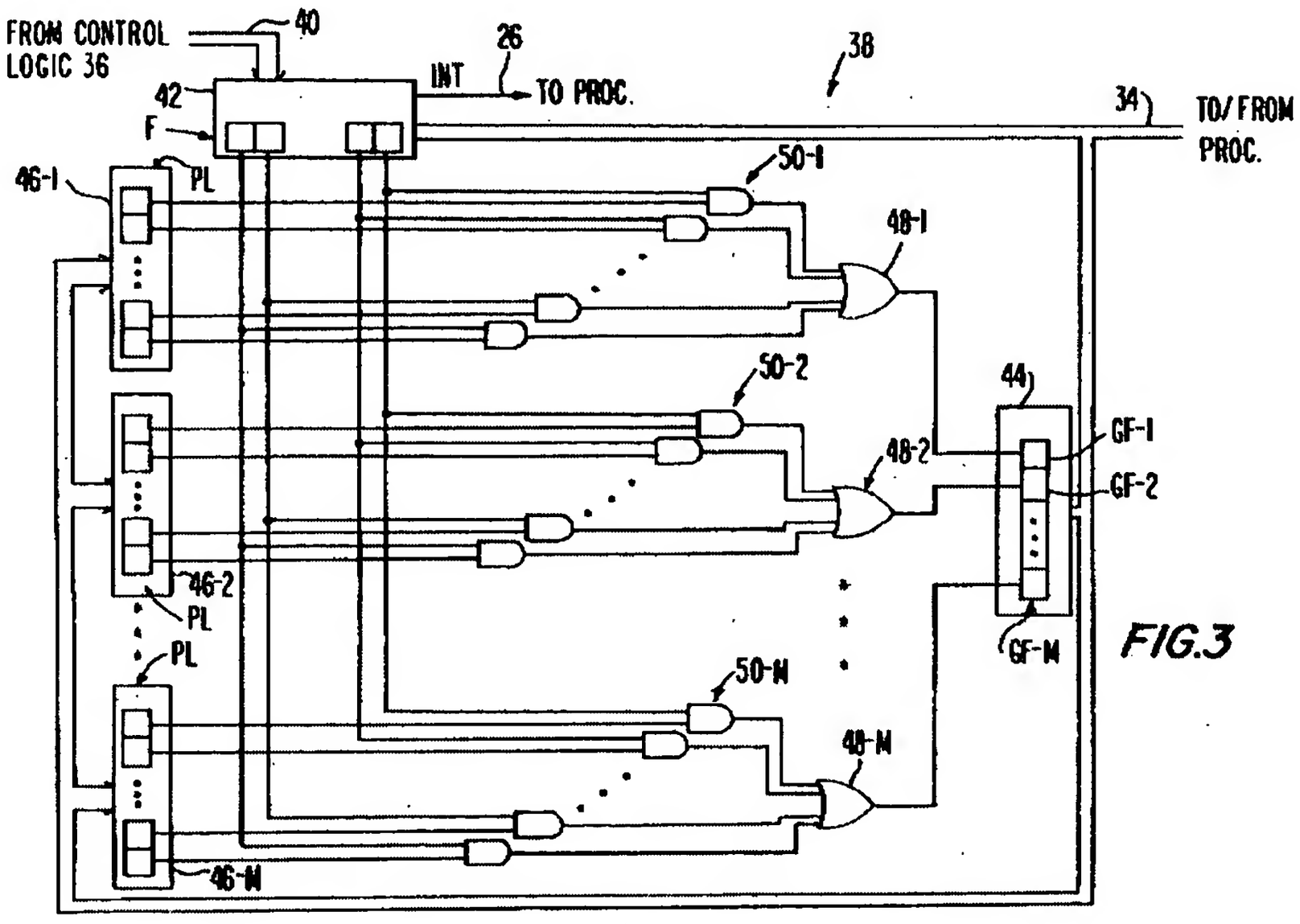


FIG.3

At the outset, in order to have a clear understanding of the following discussion, it is important to note that the interrupt requests can be generated from register 44 instead of register 42 (see column 11, lines 10-15). In addition, the term "group" used in Wash includes group that has only one interrupt resource (see column 11, lines 47-49).

As shown above and specifically described in column 4, line 63 to column 6, line 43; column 10, line 55 to column 11, line 48, the number of storage locations F in register 42 is equal to the number of interrupt sources, any one of which may cause the

transmission of the interrupt signal to processor 14. Also, the locations F correspond one-to-one to the interrupt sources. The plurality of interrupt resources are routed or mapped to a plurality of interrupt inputs represented by a plurality of locations GF; wherein the interrupt request signal generated when any one or more of the locations GF are set. Further, in Wash, a masking bit is used to enable or disable interrupt requests from each of a plurality of interrupt sources to one or more of the plurality of interrupt inputs. Specifically, when it is desired to mask a given one of the interrupt sources, processor 14 sends programming signals to the association registers 46 such that the value "0" is stored in the respective location PL corresponding to the interrupt source to be masked.

With regard to claim 2, as discussed above, when it is desired to mask a given one of the interrupt sources, processor 14 sends programming signals to the association registers 46 such that the value "0" is stored in the respective location PL corresponding to the interrupt source to be masked.

With regard to claim 3, as discussed above, when it is desired to mask a given one of the interrupt sources, processor 14 sends programming signals to the association registers 46 such that the value "0" is stored in the respective location PL corresponding to the interrupt source to be masked. Further, as also discussed above, each location PL corresponds to each of interrupt source. Thus, it is clear that a control bit value can be selectively set in each of location PL corresponding to the mapped interrupt source/interrupt input combination.

With regard to claim 4, as discussed above, the masking control bit is programmable. Thus, it is clear that the control bit values can be set according to user preferences.

With regard to claim 5, as discussed above, the masking control bit is programmable. Thus, it is clear that the control bit values can be dynamically modified according to user preferences.

With regard to claim 6, it is clear that the control bit values must be defined according to system requirements. Further, it is also clear that the system of Wash comprises the processor, at least one interrupt source, and at least one interrupt input.

With regard to claims 7-12, see discussion above, since the subject matter presented in claims 7-12 has already been addressed.

With regard to claim 13, as clearly shown in the figure above, the logic that selectively enables comprises, for each mapped interrupt source/interrupt input combination, a logical AND (50) for ANDing each interrupt source with a respective control bit value.

With regard to claim 14, Wash discloses a system for sharing a plurality of interrupt inputs associated with a processor among a plurality of interrupt sources (Wach discloses an interrupt architecture employing interrupt sharing, which is best illustrated in the following figure:

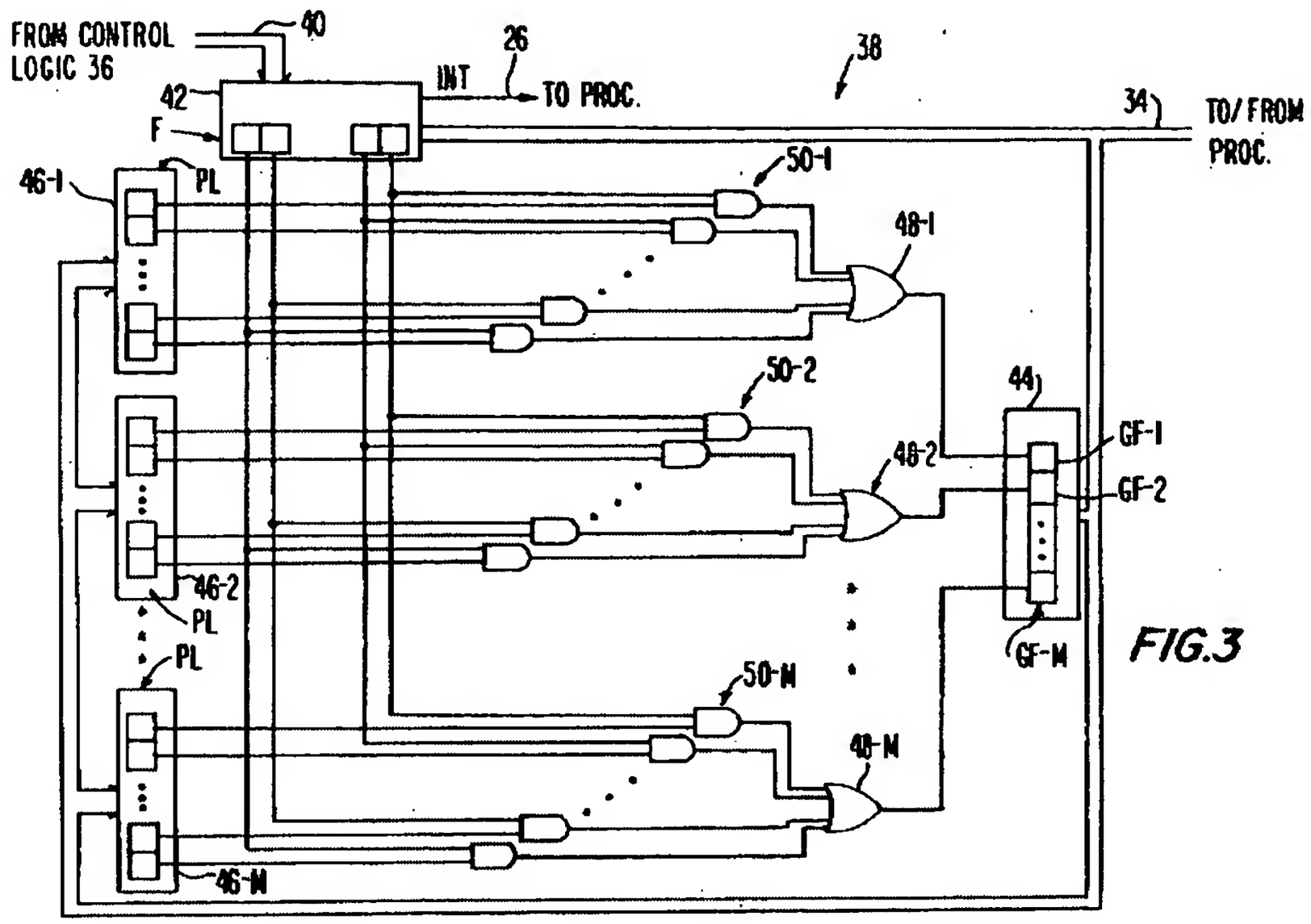


FIG.3

, comprising: for each of said plurality of interrupt inputs: a plurality of logical ANDs, each corresponding to an interrupt source, the corresponding interrupt source providing an interrupt request signal to the corresponding logical AND to interrupt the processor (a plurality of AND gates 50, each having an input to receive an interrupt request signal from an interrupt source to interrupt the processor; see also discussion above regarding claim 1); a plurality of control bits each corresponding to an interrupt source and each respectively providing a control bit value to the corresponding logical AND (a plurality of masking bits, each can be set in the location PL to provide a control value to the other input of AND gate 50; see also discussion regarding claim 1 above), wherein, based on the control bit value, a corresponding interrupt request signal is

provided at an output of the corresponding logical AND (based on the control bit value provided at one input of the AND gate, an interrupt request signal is provided at output of the AND gate 50; see also discussion above regarding claim 1); a logical OR arranged to indicate, to the interrupt input, the presence of a corresponding interrupt request signal from at least one output of the plurality of logical ANDs (as clearly discussed above regarding claim 1, the OR gate 48 is arranged to indicate the presence of a corresponding interrupt request signal from at least one output of the plurality of AND gates 50 to the interrupt input; see also discussion above regarding claim 1).

With regard to claims 15-20, see discussion above, since the subject matter presented in claims 15-20 has already been addressed.

Response to Arguments

Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

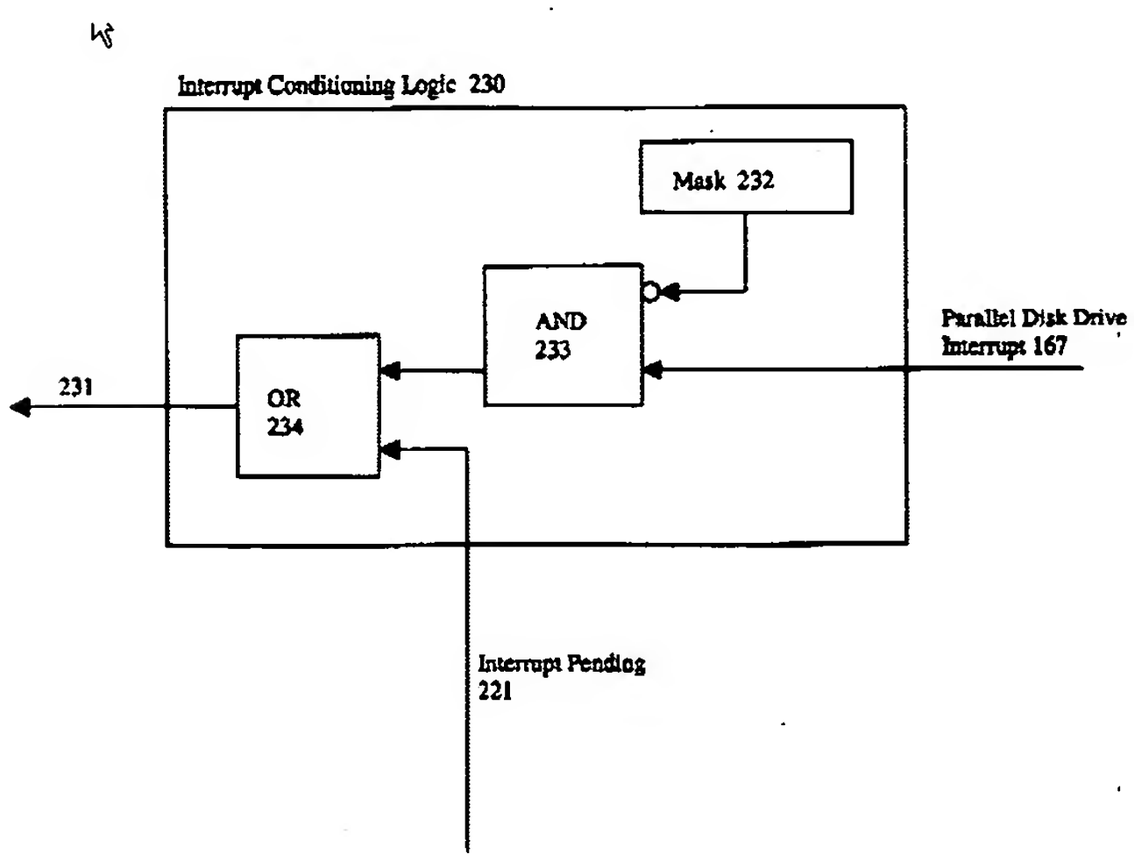
Relevant Art

US Patent Nos. 6,772,258 to Poisner et al., 6,704,823 to Perez et al., 6,401,154 to Chiu et al., 6,192,425 to Sato, 6,141,703 to Ding et al., 5,187,781 to Heath, and 4,768,149 to Konopik et al. are cited as relevant art.

US PG Pub No. 2002/0116563 to Lever is cited as relevant art.

Non Patent Literature/Printed documents: Hitachi 16-Bit Single Chip Microcomputer, section 5: Interrupt Controller, Interrupt and Controlling accessed from http://www.cs.huji.ac.il/course/2004/rtdsp/Lectures/interrupts.pdf, Adaptive Interrupt Sharing, Interrupt Sharing for Personal Computer, and Shared Planar Interrupt for Personal Computers are also cited as relevant art.

Poisner et al. discloses an interrupt sharing circuit using a combination of AND gate and OR gate, wherein one input of the AND gate is connected to a mask register for providing a enable/disable control.



Perez discloses dynamic allocation of interrupt lines through interrupt sharing.

Chiu discloses the use of interrupt sharing in PC/AT architecture using 8259A PIC.

Sato and Heath disclose interrupt line sharing circuits.

Ding discloses an interrupt sharing system to map interrupt request signals to a one of system interrupt signals based on characteristics of each peripheral device.

Konopik discloses a method of sharing a common interrupt line among a plurality of I/O devices being serviced by an interrupt handler.

Lever discloses an interrupt handling scheme in a computing apparatus having a plurality of devices that share a shared interrupt request line.

In the "Interrupt and Controlling" accessed from http://www.cs.huji.ac.il/course/2004/rtdsp/Lectures/interrupts.pdf, discloses mapping interrupt sources to CPU interrupts. "There are 16 interrupt sources, each with a selection number. The CPU, however, has 12 interrupts available for use. So an interrupt source must be mapped to a CPU interrupt. This is done by setting appropriate bits of the two memory mapped Interrupt Multiplex Registers."

No further discussion is provided for other relevant documents cited above, since they are self-explanatory.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Dang whose telephone number is 571-272-3626. The examiner can normally be reached on Monday-Friday from 9:AM to 5:PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart, can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Khanh Dang
Primary Examiner